# MILLIMETERWAVE CHARACTERISTICS OF FLIP-CHIP INTERCONNECTS FOR MULTI-CHIP MODULES

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## ABSTRACT

Electromagnetic simulations and measurement data of flip-chip transitions are presented. First-order effects are identified and design criteria for mm-wave multi-chip interconnects are derived. In coplanar environment, the flip-chip scheme provides interconnects with excellent low-reflective properties. For conductor-backed structures, the suppression of parasitic modes represents the key issue.

## INTRODUCTION

Cost-effective packaging is a precondition for the development of commercial millimeterwave systems. Among the multi-chip module schemes available, the flip-chip approach is one of the most promising ones. For single chips, excellent mm-wave properties have been demonstrated [1,2,3]. It is not clear, however, whether these results can be generalized to more complex systems and which are the design criteria. Electromagnetic modeling of flip-chip interconnects has been the subject of several publications (e.g. [4,5,6]), but a comprehensive treatment of the electromagnetic behavior in view of the practical limitations is still missing. This is the motivation for this paper.

The purpose is to provide guidelines to the design engineer what determines the mm-wave characteristics of flip-chip interconnects and how they should be designed from an electromagnetic point of view.

The results are based on extensive simulations using a 3D Finite-Difference frequency-domain (FDFD) code developed from [7] and backed by measurements of test structures.

## THE INFLUENCE OF FLIP-CHIP MOUNTING ON ELECTRICAL PERFORMANCE

### Detuning and Bump Height

The first important parasitic effect introduced by flip-chip mounting is detuning of the chip. Due to flipping, the surface of the motherboard is near to the elements on the chip surface with the distance being approximately the bump height. This changes the electrical characteristics of the on-chip elements, which is especially pronounced for transmission lines. One has to distinguish whether a metallization is present on the motherboard below the chip or not. Fig. 1 illustrates the resulting deviations for a typical coplanar waveguide with 50µm ground-to-ground spacing on GaAs.

From the data in Fig. 1 one concludes that any metallization underneath the flipped chip has a significant influence. For the non-metallized case, bump heights in the order of 20µm lead to deviations below 2%, which usually can be tolerated. Using a metallized motherboard surface, however, one requires considerably larger heights in order to prevent severe detuning. Then, on technological reasons, the bump cross-sectional dimensions have to be increased accordingly since bump aspect-ratio is fixed. As a consequence, pad size grows as well and the high-frequency performance deteriorates. The data in Fig. 1 refers to a 50µm wide CPW on the chip. When increasing ground-to-ground spacing or when using microstrip lines instead of CPW one obtains even larger deviations. Hence, from the

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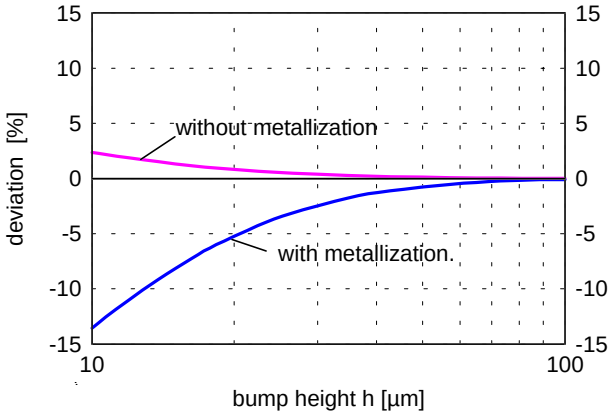
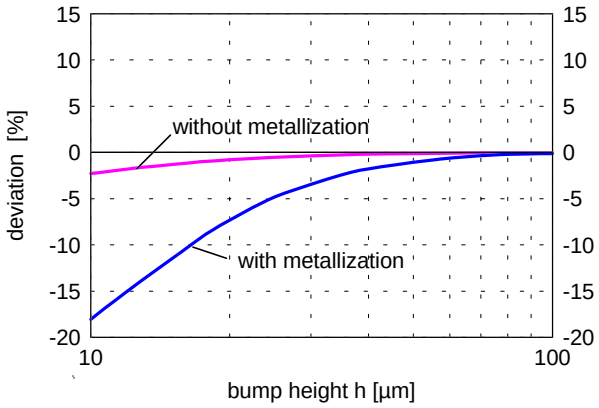
electromagnetic point of view, the non-metallized case shows clear advantages.




a) Phase constant β




b) Characteristic impedance Z

Fig. 1 Deviations of CPW transmission-line parameters as a function of flip-chip bump height h for the case with and without metallization on the surface of the motherboard below the chip (50Ω CPW with 50µm ground-to-ground spacing on GaAs).

Scattering Behavior of the Interconnect

In this subsection, a single transition from CPW on the motherboard to a coplanar line on the flipped chip is considered. The question is how bump geometry influences reflection of the transition. Figs. 2 and 3 present 3D electromagnetic simulation results. In Fig. 2, the parameter is bump height, in Fig. 3, bump length (i.e., the bump dimension in propagation direction) is varied.

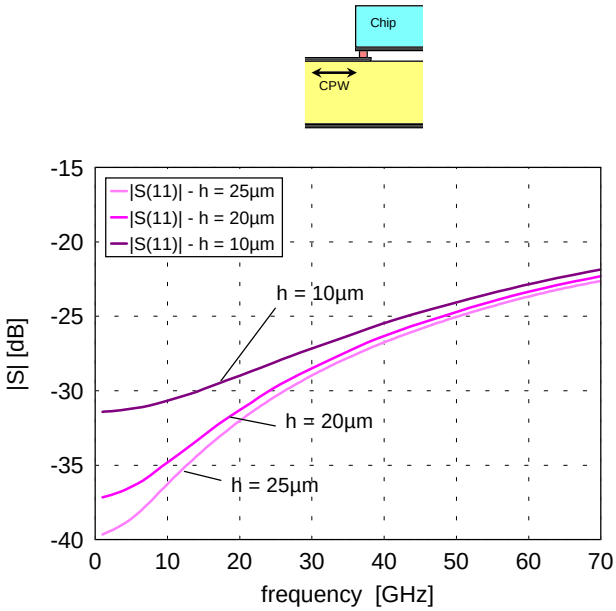



Fig. 2 Reflection coefficient of a single flip-chip transition as a function of frequency with the bump height h as parameter (50Ω CPW with 120µm ground-to-ground spacing on motherboard and chip, bump cross-section is 25 x 25 µm²).

The unexpected finding is that bump length is the most important parameter in the mm-wave frequency range while bump height does not influence reflection significantly (the differences at lower frequencies are caused by detuning effects mentioned above and not by the parasitics of transition itself). Further investigations reveal that the transition shows a capacitive behavior and not an inductive one as might be expected when describing the bump section by a three-conductor line in air (e.g. [5]).

Quantitatively, the return loss data in Figs. 2 and 3 are excellent and demonstrate the potential of the flip-chip technique for mm-wave applications. When evaluating practical relevance, however, the transitions have to be considered together with the motherboard packaging scheme.

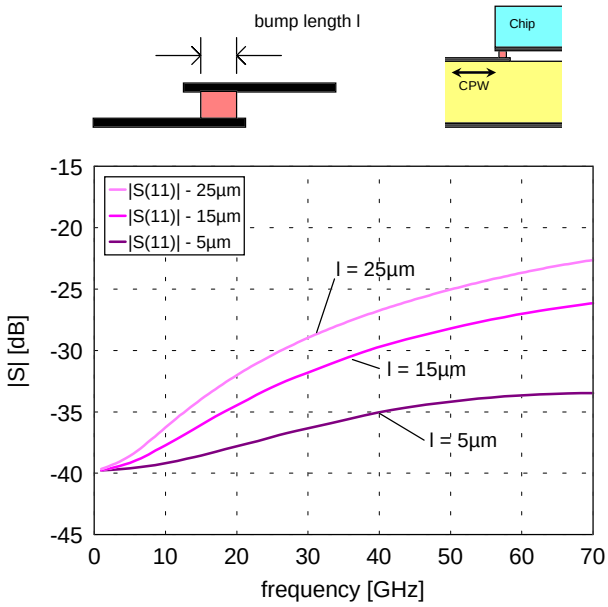



Fig. 3 Reflection coefficient of a single flip-chip transition against frequency with the bump length l as parameter (l denotes the bump dimension in propagation direction, bump height and width: 25µm, other data as in Fig. 2).

## PARASITIC MODES

Besides the reflection properties of the CPW mode, the existence of parasitic substrate modes in the motherboard must be accounted for. For the flip-chip scheme, one has mainly two types of parasitic modes:

- When using a metallized motherboard surface below the chip, an additional parallel-plate mode exists in the air region between the two substrates (see also [6]). This causes parasitic coupling and half-wavelength resonances. In Fig. 4, measurement and simulation results for a test structure are given. As expected, one observes parasitic resonances, which cause reflection coefficient values of -10dB already at 10 GHz.

- In common packaging set-ups, the backside of the motherboard is conducting. The conductor is formed either by backside metallization or by the bottom plane of the package. Therefore, a parasitic parallel-plate mode is propagating in the motherboard. This reduces isolation between ports (see also [8]), which may cause severe circuit instabilities. There is no easy way to suppress this mode. Further work on this subject is in progress.

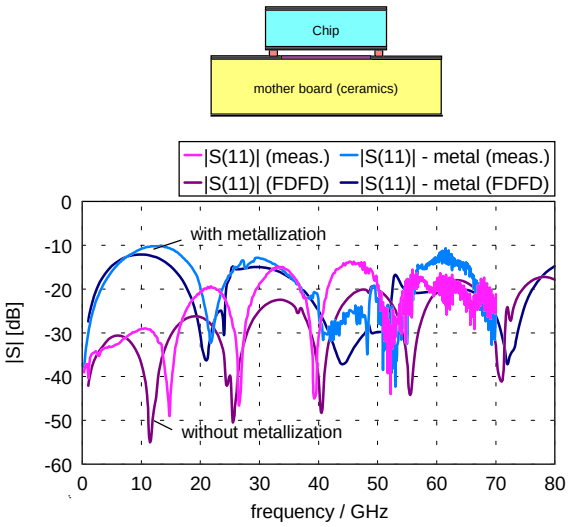



Fig. 4 Reflection due to flip-chip mounting against frequency: measurements and FDFD simulation data for the case with and without metallization on the motherboard surface below the chip; the chip contains a CPW through-line (bump height 25µm, chip length 4.2 mm, other data as in Fig. 2).

## SIMPLIFIED MODELLING

Based on the FDFD simulations, simplified models for the flip-chip transition can be developed. Because of the high return loss, simple models yield sufficient accuracy for circuit design. The results in Figs. 2 and 3, for instance, can be described by a lumped shunt capacitance at the transition.

In order to determine parasitic-mode coupling, the method of [8] can be applied. Using this approach, one obtains accurate information without computationally expensive 3D calculations.

## CONCLUSIONS

Electromagnetic simulation of the flip-chip transition yields some important design criteria for multi-chip module schemes:

- Metallization on the motherboard below the chip should be avoided. For common bump heights below 25µm, it causes severe detuning and parasitic half-wavelength resonances.

- In a coplanar environment, the reflection characteristics of the bump structure itself are excellent up to the mm-wave range. First-order parameter is the longitudinal dimension of the bumps, not the bump height. The influence of the cross-sectional shape (rectangular, circular or elliptical) is of minor importance and can be adapted to the fabrication process. A simplified description of the transition by a lumped capacitance is possible.

- The most serious problem is the existence of parasitic modes for a conductor-backed motherboard. The additional mode gives rise to coupling and resonances between ports, especially in the mm-wave range, where chip dimensions exceed half the wavelength. Shorting bumps represent a possible solution, but further work on this issue is necessary.

## ACKNOWLEDGEMENTS

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